INSTRUCTION PROCESSOR EMULATOR HAVING SEPARATE OPERAND AND OP-CODE INTERFACES

ABSTRACT

Techniques are described for emulating an instruction processor for use during the development of a computer system. Specifically, the techniques describe an emulated instruction processor that accurately and efficiently emulates an instruction processor having separate interfaces to fetch op-codes and operands. Further, the emulated instruction processor may provide detection of errors associated with the separate interfaces. By making use of the techniques described herein, detailed information relating to errors associated with the memory architecture may be gathered for use in verifying components within the memory architecture, such as first and second-level caches.